

WHAT IS CLAIMED IS:

- 1 1. A transistor, comprising:
2 a workpiece, the workpiece comprising a top surface;
3 a crystalline implantation region disposed within the workpiece, the crystalline
4 implantation region comprising germanium, wherein the crystalline implantation region extends
5 within the workpiece from the top surface of the workpiece by about 120 Å or less;
6 a gate dielectric disposed over the crystalline implantation region;
7 a gate disposed over the gate dielectric; and
8 a source region and a drain region formed in at least the crystalline implantation region
9 within the workpiece.
- 1 2. The transistor according to Claim 1, wherein the crystalline implantation region
2 comprises a concentration of about 1×10^{17} to about 5×10^{23} atoms/cm³ of germanium.
- 1 3. The transistor according to Claim 1, wherein the crystalline implantation region
2 comprises a top portion comprising about 50% or greater of germanium.
- 1 4. The transistor according to Claim 3, wherein the crystalline implantation region top
2 portion comprises substantially 100% germanium.
- 1 5. The transistor according to Claim 3, wherein the crystalline implantation region top
2 portion comprises a thickness of about 20 Å.
- 1 6. The transistor according to Claim 1, wherein the gate dielectric comprises a material
2 having a dielectric constant of about 4.0 or greater.

- 1 7. The transistor according to Claim 6, wherein the gate dielectric comprises HfO_2 , HfSiO_x ,
2 Al_2O_3 , ZrO_2 , ZrSiO_x , Ta_2O_5 , La_2O_3 , Si_xN_y , SiON , or combinations thereof.
- 1 8. The transistor according to Claim 1, wherein the gate dielectric comprises SiO_2 .
- 1 9. The transistor according to Claim 1, further comprising isolation regions disposed in the
2 workpiece, and further comprising spacers formed over and abutting sidewalls of the gate and
3 gate dielectric.
- 1 10. The transistor according to Claim 1, wherein the workpiece comprises a silicon-on-
2 insulator (SOI) wafer.

1 11. A method of fabricating a transistor, the method comprising:
2 providing a workpiece, the workpiece having a top surface;
3 implanting germanium into the top surface of the workpiece, forming a first germanium-
4 containing region within the top surface of the workpiece and forming a second germanium-
5 containing region beneath the first germanium-containing region, the first germanium-containing
6 region extending a first depth beneath the workpiece top surface, the second germanium-
7 containing region having a second depth extending below the first depth, the first and second
8 depth comprising about 100 Å or less below the top surface of the workpiece;
9 depositing a gate dielectric material over the first germanium-containing region;
10 depositing a gate material over the gate dielectric material;
11 patterning the gate material and gate dielectric material to form a gate and a gate
12 dielectric over the first germanium-containing region; and
13 forming a source region and a drain region in at least the first germanium-containing
14 region.

1 12. The method according to Claim 11, wherein forming the first germanium-containing
2 region comprises forming an amorphous germanium-containing region, and wherein forming the
3 second germanium-containing region comprises forming a first crystalline germanium-
4 containing region.

1 13. The method according to Claim 12, further comprising annealing the workpiece, before
2 depositing the gate dielectric material, converting the amorphous germanium-containing region
3 to a second crystalline germanium-containing region, the first crystalline germanium-containing
4 region and the second crystalline germanium-containing region comprising a single crystalline
5 germanium-containing region, the single crystalline germanium-containing region comprising a
6 third depth beneath the workpiece top surface.

1 14. The method according to Claim 13, wherein the third depth is about 120 Å or less.

1 15. The method according to Claim 13, wherein the first depth is about 45 Å or less, and the
2 second depth is about 55 Å or less.

1 16. The method according to Claim 13, wherein annealing the workpiece comprises heating
2 the workpiece to a temperature of about 750 °C or less for about 60 minutes or less.

1 17. The method according to Claim 12, further comprising annealing the workpiece, after
2 depositing the gate dielectric material, converting the amorphous germanium-containing region
3 to a second crystalline germanium-containing region, the first crystalline germanium-containing
4 region and the second crystalline germanium-containing region comprising a single crystalline
5 germanium-containing region, the single crystalline germanium-containing region comprising a
6 third depth beneath the workpiece top surface.

1 18. The method according to Claim 17, wherein the third depth is about 120 Å or less.

1 19. The method according to Claim 17, wherein the first depth is about 45 Å or less, and the
2 second depth is about 55 Å or less.

1 20. The method according to Claim 17, wherein annealing the workpiece comprises heating
2 the workpiece to a temperature of about 750 °C or less for about 60 minutes or less.

1 21. The method according to Claim 12, wherein implanting germanium into the top surface
2 of the workpiece comprises forming a damage region between the first germanium-containing
3 region and the second germanium-containing region, further comprising annealing the
4 workpiece, converting the amorphous germanium-containing region to a second crystalline
5 germanium-containing region, the first crystalline germanium-containing region and the second
6 crystalline germanium-containing region comprising a single crystalline germanium-containing
7 region, and wherein annealing the workpiece causes the removal of the damaged region between
8 the first germanium-containing region and the second germanium-containing region.

1 22. The method according to Claim 11, wherein implanting the germanium comprises
2 implanting germanium at an energy dose of about 5 keV or less.

1 23. The method according to Claim 11, wherein implanting the germanium comprises
2 implanting germanium at a dose of about 1×10^{15} to 1×10^{17} atoms/cm².

1 24. The method according to Claim 11, wherein implanting the germanium comprises
2 forming the first germanium-containing region comprising at least 80% germanium at a top
3 portion thereof.

1 25. The method according to Claim 24, wherein implanting the germanium comprises
2 forming the first germanium-containing region comprising substantially 100% germanium at a
3 top portion thereof.

- 1 26. The method according to Claim 11, wherein depositing the gate dielectric material
2 comprises depositing a material having a dielectric constant of about 4.0 or greater.
- 1 27. The method according to Claim 26, wherein the depositing the gate dielectric material
2 comprises depositing HfO_2 , HfSiO_x , Al_2O_3 , ZrO_2 , ZrSiO_x , Ta_2O_5 , La_2O_3 , Si_xN_y , SiON , or
3 combinations thereof.
- 1 28. The method according to Claim 11, wherein depositing the gate dielectric material
2 comprises depositing SiO_2 .
- 1 29. The method according to Claim 11, further comprising forming isolation regions in the
2 workpiece, before implanting germanium into the top surface of the workpiece.
- 1 30. The method according to Claim 11, further comprising forming spacers over sidewalls of
2 the gate and gate dielectric.
- 1 31. The method according to Claim 11, wherein providing the workpiece comprises
2 providing a silicon-on-insulator (SOI) wafer.
- 1 32. The method according to Claim 11, wherein forming the source and drain regions
2 comprises a temperature of about 938.3°C or less.

33. A method of fabricating a transistor, the method comprising:

providing a workpiece, the workpiece having a top surface;

implanting germanium into the top surface of the workpiece, forming an amorphous germanium-containing region within the top surface of the workpiece, the amorphous germanium-containing region extending about 45 Å or less beneath the workpiece top surface, wherein implanting germanium into the top surface of the workpiece also forms a first crystalline germanium-containing region beneath the amorphous germanium-containing region, the first crystalline germanium-containing region extending about 55 Å or less beneath the amorphous germanium-containing region;

depositing a gate dielectric material over the amorphous germanium-containing region, the gate dielectric material having a dielectric constant of about 4.0 or greater;

annealing the workpiece at a temperature of about 750 °C or less for about 60 minutes or less, re-crystallizing the amorphous germanium-containing region and forming a single second crystalline germanium-containing region within the top surface of the workpiece, the single second crystalline germanium-containing region comprising the re-crystallized amorphous germanium-containing region and the first crystalline germanium-containing region, the second crystalline germanium-containing region extending about 120 Å or less beneath the workpiece top surface;

depositing a gate material over the gate dielectric material;

patterning the gate material and gate dielectric material to form a gate and a gate dielectric over the second crystalline germanium-containing region; and

forming a source region and a drain region in at least the second crystalline germanium-containing region.

1 34. The method according to Claim 33, wherein implanting the germanium into the top
2 surface of the workpiece comprises forming a damage region between first germanium-
3 containing region and the second germanium-containing region, further comprising annealing the
4 workpiece, converting the amorphous germanium-containing region to a second crystalline
5 germanium-containing region, the first crystalline germanium-containing region and the second
6 crystalline germanium-containing region comprising a single crystalline germanium-containing
7 region, and wherein annealing the workpiece causes the removal of the damaged region between
8 the first germanium-containing region and the second germanium-containing region.

1 35. The method according to Claim 33, wherein implanting the germanium comprises
2 implanting germanium at an energy dose of about 5 keV or less and at a dose of about 1×10^{15} to
3 1×10^{17} atoms/cm².

1 36. The method according to Claim 33, wherein implanting the germanium comprises
2 forming the first germanium-containing region comprising at least 50% germanium at a top
3 portion thereof.

1 37. The method according to Claim 33, wherein the depositing the gate dielectric material
2 comprises depositing HfO₂, HfSiO_x, Al₂O₃, ZrO₂, ZrSiO_x, Ta₂O₅, La₂O₃, Si_xN_y, SiON, or
3 combinations thereof.

1 38. The method according to Claim 33, wherein forming the source and drain regions
2 comprises a temperature of about 938.3 °C or less.